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REMARKS/ARGUMENTS

In the outstanding Final Office Action, claims 42-57 were examined. Claims 42-57 were rejected. In response to the above identified Final Office Action, Applicants amend claims 45, 48 and 54 and cancel claim 57. Entry of the amendments is respectfully requested. Applicants respectfully request reconsideration in view of the aforementioned amendment and the following remarks.

I. In the Drawings

Examiner objects to the drawings under 37 CFR 1.83(a) because the drawings must show every feature of the invention specified in the claims. Specifically, Examiner states that elements recited in claims 48, 54 and 57 are not shown in the drawings. In response, Applicants amend claims 48 and 54 and cancel claim 57. Specifically, the support for claim 48 can be found in Figures 4A and 4B of the Drawings (*see also* explanation below). Consequently, Applicants respectfully request reconsideration and withdrawal of the objections to claims 48, 54 and 57.

II. Claim Objection

A. Examiner objects to claim 54 due to certain informalities. In response, Applicants amend claim 54 to recite "*the* two of the firmware modules are to be dispatched" to comply with Examiner's request. Consequently, Applicants respectfully request reconsideration and withdrawal of the objection to claim 54.

III. Claims Rejected Under 35 U.S.C. § 112, first and second paragraphs

A. Examiner rejects claim 48 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Specifically, Examiner has focused on the "third module" recited in the claim, and notes that there is no discussion of "when the third firmware module is dispatched subsequent to the two initial firmware modules." Applicants respectfully point out that claim 48 does not recite dispatching the third firmware module *subsequent to* the first two modules. Rather, the third module is dispatched *before* one of the first two modules calls a function in the third module. Applicants acknowledge the potential for confusion regarding dispatch order posed by identifying the module as the *third* module, and so propose

calling this module the *service-exporting module*, as recited in the amended claims. Support for this name is at p. 10, ll. 19-27. Reconsideration and withdrawal of this rejection are respectfully requested.

B. Examiner rejects claim 57 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Claim 57 is canceled without prejudice. Accordingly, this rejection is moot.

IV. Claims Rejected Under 35 U.S.C §102(e)

Examiner rejects claims 42 and 48 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,633,976 issued to Stevens ("Stevens"). To anticipate a claim, Examiner must show that a single reference teaches each of the elements of that claim, arranged as recited in the claim.

Independent claim 42 recites a method comprising several operations, all of which are to occur *before* a final operation of initializing a system memory. This is the essence of the "Pre-Memory Execution Environment" in this Application's title. As described in the Specification at p.7, line 17 through p.8, line 9, a computer system performs various self-test and initiation operations when it starts up *before* the system memory (e.g. DRAM) is initialized and made available for use. Stevens, on the other hand, dispatches its BIOS modules into the system memory only *after* the system memory are initialized (Stevens, column 5, lines 27-43). The dissimilarity in whether to initialize system memory before or after the firmware modules are dispatched is the reason that Stevens does not teach each of the elements of claim 42.

As a result, Examiner's assertion that "two firmware modules" in claim 42 is anticipated by a module to initialize CPU and a module to initialize memory lacks concrete support. In Stevens, a minimal initialization code that initializes both the CPU and the memory is executed *before* the plurality of BIOS modules are dispatched (Stevens, column 3, lines 1-15). In contrast, "initializing a system memory *after* dispatching the two firmware modules," as recited in claim 42, clearly shows that the two firmware modules are dispatched *before* any system memory is initialized. Consequently, Stevens fails to teach each of the elements of claim 42.

In regard to claim 48, this claim depends from base claim 42 and thus incorporates the limitations thereof. For at least the reasons stated above in regard to claim 42, Stevens does not teach each of the elements of claim 48. Consequently, Applicants respectfully submit that claims 42 and 48 are allowable over the reference of record.

V. Claims Rejected Under 35 U.S.C. § 103(a)

A. Examiner rejects claims 43 and 44 under 35 U.S.C.§103(a) as being unpatentable over Stevens in view of U. S. Patent No. 5,999,989 issued to Patel ("Patel"). To establish a *prima facie* case of obviousness, Examiner must show that the cited references teach or suggest each element of the claim.

In regard to claims 43 and 44, these claims depend from base claim 42 and thus incorporate the limitations thereof. For at least the reasons stated above in regard to claim 42, Stevens does not teach or suggest each of the elements of claims 43 and 44. Further, Patel does not cure the defects of Stevens. Examiner has not relied upon and Applicants have been unable to discern any part of Patel that teaches or suggests "initializing a system memory after dispatching the two firmware modules," as recited in claim 42. Thus, the references of record fail to teach or suggest each of the elements of claims 43 and 44, even assuming (solely for the sake of argument) that the references could properly be combined. As a result, Applicants respectfully submit that claims 43 and 44 are allowable over the references of record.

B. Examiner rejects claims 45-47 under 35 U.S.C. § 103(a) as being unpatentable over Stevens in view of U. S. Patent 6,353,924 issued to Ayers et al. ("Ayers").

In regard to claims 45-47, these claims depend from base claim 42 and thus incorporate the limitations thereof. For at least the reasons stated above in regard to claim 42, Stevens does not teach or suggest each of the elements of claims 45-47. Further, Ayers does not cure the defects of Stevens. Examiner has not relied upon and Applicants have been unable to discern any part of Ayers that teaches or suggests "initializing a system memory after dispatching the two firmware modules," as recited in claim 42. Thus, the references of record fail to teach or suggest each of the elements of claims 45-47, even assuming (solely for the sake of argument)

that the references could properly be combined. As a result, Applicants respectfully submit that claims 45-47 are allowable over the references of record.

C. Examiner rejects claim 49 under 35 U.S.C. § 103(a) as being unpatentable over Stevens in view of U. S. Publication 2001/0007119 to Katayama, et al ("Katayama").

In regard to claim 49, this claim depends from base claim 42 and thus incorporates the limitations thereof. For at least the reasons stated above in regard to claim 42, Stevens does not teach or suggest each of the elements of claim 49. Further, Katayama does not cure the defects of Stevens. Examiner has not relied upon and Applicants have been unable to discern any part of Katayama that teaches or suggests "initializing a system memory after dispatching the two firmware modules," as recited in claim 42. Thus, the references of record fail to teach or suggest each of the elements of claim 49, even assuming (solely for the sake of argument) that the references could properly be combined. As a result, Applicants respectfully request that claim 49 be allowed over the references of record.

D. Examiner rejects claims 50, 51 and 53 under 35 U.S.C. § 103(a) as being unpatentable over Patel.

Patel teaches an invention to enhance the robustness of the Plug-and-Play BIOS and reduces the amount of ROM required to support different devices in a computer (Patel, Abstract). Among other things, Examiner admits that Patel does not explicitly teach "initializing a volatile system memory after dispatching the plurality of firmware modules," as recited in claim 50. To cover the deficiency of Patel, Examiner states that it would have been obvious to one of ordinary skill in the art to have the volatile system memory initialized after dispatching the plurality of firmware modules. The motivation is to conserve memory resources (Office Action, p.9, lines 2-4). This statement is unsupported by any prior art, and is contradicted by Stevens. Above all, the system memory in Stevens is initialized *before* the memory modules are dispatched (Stevens, column 3, lines 27-43). In contrast, claim 50 discloses "initializing a volatile system memory *after* dispatching the plurality of firmware modules," which teaches the opposite order. Since Patel does not state explicitly regarding whether to dispatch memory modules before system memory initialization or after system memory initialization, and since Stevens teaches initializing system memory *before* the memory modules are dispatched, Examiner's statement

that one of ordinary skill in the art would be motivated to have the volatile system memory initialized *after* dispatching the plurality of firmware modules is unsupported.

In regard to claims 51 and 53, these claims depend from base claim 42 and thus incorporate the limitations thereof. For at least the reasons stated above in regard to claim 50, Patel does not teach or suggest each of the elements of claims 51 and 53. As a result, Applicants respectfully request that claims 50, 51 and 53 be allowed over the reference of record.

E. Examiner rejects claim 52 under 35 U.S.C. § 103(a) as being unpatentable over Patel in view of Ayers.

In regard to claim 52, this claim depends from base claim 50 and thus incorporates the limitations thereof. For at least the reasons stated above in regard to claim 50, Patel does not teach or suggest each of the elements of claim 52. Further, Ayers does not cure the defects of Patel. Examiner has not relied upon and Applicants have been unable to discern any part of Ayers that teaches or suggests "initializing a volatile system memory *after* dispatching the plurality of firmware modules," as recited in claim 50. Thus, the references of record fail to teach or suggest each of the elements of claim 52, even assuming (solely for the sake of argument) that the references could properly be combined. As a result, Applicants respectfully request that claim 52 be allowed over the references of record.

F. Examiner rejects claims 54-56 rejected under 35 U.S.C. § 103(a) as being unpatentable over Stevens in view of Patel.

In regard to independent claim 54, Stevens does not teach or suggest "the two of the firmware modules are to be dispatched before the volatile memory is initialized," as recited in claim 54, for the analogous reasons stated above in regard to claim 42. Further, Patel does not cure the defects of Stevens. As discussed above in regard to claim 50, Patel fails to teach or suggest "the two of the firmware modules are to be dispatched before the volatile memory is initialized," as recited in claim 54.

With respect to claims 55 and 56, these claims depend from base claim 54 and thus incorporate the limitations thereof. For at least the reasons stated above in regard to claim 54, Stevens in view of Patel does not teach or suggest each of the elements of claims 55 and 56, even

assuming (solely for the sake of argument) that the references could properly be combined. As a result, Applicants respectfully request that claims 54-56 be allowed over the references of record.

G. Examiner rejects claim 57 under 35 U.S.C. § 103(a) as being unpatentable over Stevens and Patel and further in view of U. S. Patent 6,173,350 issued to Hudson et al. ("Hudson").

In regard to claim 57, this claim depends from base claim 54 and thus incorporates the limitations thereof. For at least the reasons stated above in regard to claim 54, Stevens in view of Patel fails to teach or suggest each of the elements of claim 57. Further, Hudson fails to cure the defects of Stevens and Patel. Examiner has not relied upon and Applicants have been unable to discern any part of Hudson that teaches or suggests "the two of the firmware modules are to be dispatched before the volatile memory is initialized," as recited in claim 54, even assuming (solely for the sake of argument) that the references could properly be combined. As a result, Applicants respectfully request that claim 57 be allowed over the references of record.

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CONCLUSION

In view of the foregoing, it is submitted that the pending claims patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: February 21, 2007

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this paper is being transmitted by facsimile on the date shown below to the United States Patent and Trademark Office.

Jean Svoboda February 21, 2007